Please amend the paragraph from page 4, lines 3 to 11, as follows:

Note that the AMELD pixel always operates digitally even when displaying gray-scale information. All transistors are either fully-on or fully-off and dissipate no power in either state. When a pixel is off, it simply acts as if it is disconnected from the resonant power source and therefore doesn't dissipate or waste any power. The AMELD therefore steers almost 100% of the power from the high voltage source into the activated into the activated EL cells for light generation. FIG. 7 depicts an illustrative timing relationship of the signals used for gray scale control including a frame time, a plurality of LOAD and ILLUMINATE periods, a drive current, data signals, a linear ramp control signal and a stepped control signal.

Please amend the paragraph from page 4, lines 40 to 48, as follows:

The second transistor operates as a means for controlling the current through an electroluminescent cell. The gate is either on or off during the ILLUMINATE periods but gray scale information is provided by limiting the total energy supplied to the pixel. This is done by varying the length of time this second transistor is on during the ILLUMINATE period or by varying the number of ILLUMINATE pulses emitted during an ILLUMINTE period. FIG. 8 depicts an illustrative timing relationship of the signals used for digital gray scale control including a frame time, a plurality of LOAD and ILLUMINATE periods, a drive current, data signal and a stepped control signal.

IN THE CLAIMS

Kindly add to the original patented text, as proposed in the previous responses, new claims 8, 10-12, 14-16, 20, 22, 25, 27, and 30-32 as follows:

8. In an electroluminescent display comprising an array of pixels, where each pixel contains a circuit for controlling application of energy to an electroluminescent cell associated with each pixel in said array of pixels, a method of providing gray scale illumination during a frame time comprising the steps of:

subdividing said frame time into a plurality of LOAD periods and a plurality of ILLUMINATE periods;

loading, during each LOAD period, data from a data line into said circuit; and

varying, during each of said ILLUMINATE periods, a voltage on the data line, to selectively illuminate said electroluminescent cell in response to said voltage and said data.

~~10~~ 9. The method of claim 8 wherein said voltage on said data line is a linear ramp.

~~11~~ 10. The method of claim 8 wherein said voltage on said data line is a step function.

~~12~~ 11. The method of claim 8 wherein, during each ILLUMINATE period, a high voltage power supply applies at least one pulse to said circuit and, in response to said voltage, said at least one pulse is applied to said electroluminescent cell.

~~14~~ 12. An electroluminescent display comprising an array of pixels for providing gray scale illumination during a frame time, where

said frame time is divided into a number of LOAD and ILLUMINATE periods, each pixel comprising:

a first transistor and a second transistor;

said first transistor having a first transistor gate, a first transistor source and a first transistor drain, where said first transistor gate is connected to a select line, said first transistor source is connected to a data line and said first transistor drain is connected to a second transistor gate of said second transistor;

said second transistor having said second transistor gate, a second transistor source and a second transistor drain, where said second transistor source is connected to said data line and second transistor drain is connected to an electroluminescent cell;

during each of said LOAD periods and when a select line signal on the select line activates the first transistor, said data line supplies, through said first transistor, a data signal to the second transistor gate where said data signal is stored; and

during each of said ILLUMINATE periods, said data line supplies a voltage to said second transistor to control illumination of said electroluminescent cell.

~~15~~ 13. The display of claim ~~14~~ 12 wherein said voltage is a linear ramp.

~~16~~ 14. The display of claim ~~14~~ 12 wherein said voltage is a step function.

~~20~~ 15. An electroluminescent display comprising an array of pixels for providing gray scale illumination during a frame time, where said frame time is divided into a number of LOAD and ILLUMINATE periods, each pixel comprising:

a control circuit, connected to a select line, a data line and a first electrode of an electroluminescent cell, for selectively applying energy to said electroluminescent cell in response to signals carried by said select line and said data line;

during each of said LOAD periods and when a select line signal on the select line activates the control circuit, said data line supplies a data signal to the control circuit where said data signal is stored; and

during each of said ILLUMINATE periods, in response to a state of said stored data signal, said control circuit applies pulsed energy from a power supply means to a second electrode of said electroluminescent cell for a particular period of time.

~~22.~~ 16 The display of claim ~~20~~ 15 wherein a number of ILLUMINATE periods and LOAD periods that are used to illuminate said electroluminescent cell during a frame time is equivalent to a number of bits used to define a number of levels of gray.

~~25.~~ 17 The display of claim ~~20~~ 15 wherein said control circuit further comprises:

a first transistor and a second transistor;

said first transistor having a first transistor gate, a first transistor source and a first transistor drain, where said first transistor gate is connected to a select line, said first transistor source is connected to a data line and said first transistor drain is connected to a second transistor gate of said second transistor; and

said second transistor having said second transistor gate, a second transistor source and a second transistor drain, where said second transistor source is connected to said data line and second

transistor drain is connected to a first electrode of an electroluminescent cell.

27. 18 The display of claim 20 15 wherein a number of ILLUMINATE periods and LOAD periods that are used to illuminate said electroluminescent cell during a frame time is equivalent to a number of bits used to define a number of levels of gray.

30. 19 An electroluminescent display comprising an array of pixels, each pixel comprising:

a first transistor, a second transistor and an electroluminescent cell;

said first transistor having a first transistor gate connected to a select line, a first transistor source connected to a data line, and a first transistor drain connected to a second transistor gate of said second transistor;

said second transistor having a second transistor source connected to said select line and a second transistor drain coupled to a first electrode of said electroluminescent cell; and

said electroluminescent cell having a second electrode coupled to means for providing an alternating current to the electroluminescent cell.

31. 20 The display of claim 30 19 further comprising:

a first capacitor, connected between said second transistor drain and said first electrode of said electroluminescent cell, for coupling said second transistor to said electroluminescent cell.

32. 21 The display of claim 30 19, further comprising:

a second capacitor, connected between said second electrode of said electroluminescent cell and said means for providing an